PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Keeth et al.

Serial No.: 08/530,661

Filed: September 20, 1995

For: SEMICONDUCTOR MEMORY CIRCUITRY

Confirmation No.: 5492

Examiner: E. Montalvo

Group Art Unit: 2814

Attorney Docket No.: 2269-5990US (1995-0424.00/US)

VIA ELECTRONIC FILING
August 17, 2009

BRIEF ON APPEAL

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Board of Patent Appeals and Interferences

Sirs:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc., the assignee of the pending application as recorded at Reel 7671, Frame 0965 with the United States Patent and Trademark Office.

(2) RELATED APPEALS AND INTERFERENCES

A prior appeal was filed on this application (Appeal No. 2007-3528). The Appeal Brief was filed on July 14, 2004, and the decision was made by the Board of Patent Appeals and Interferences on May 14, 2008. The appeal concerned claims 6-10, 18, 19, 22, 23, 25, and 26 which are canceled in the present application.

Neither Appellant, Appellant's representative, nor Assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF THE CLAIMS

Claims 28-31, and 34-47 are pending in the application.

Claims 1-27, and 32-33 have been previously canceled.

Claims 37-47 have been previously withdrawn.

Claims 28-31, and 34-36 stand rejected.

No claims are allowed.

The rejections of claims 28-31 and 34-36 are being appealed.

(4) STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed on April 9, 2009. On December 17, 2009, the Appellants filed an Amendment and remarks under 37 C.F.R. § 1.116 in response to the Examiner's remarks in the Final Office Action of September 18, 2008. Amendments to the claims and title were proposed in the Amendment. The Final Office Action mailed on April 9, 2009 acknowledged the Amendment and entered the amendments into the record. The Final Office Action of April 9, 2009 found the Appellants' arguments in the Remarks unpersuasive and maintained the rejection of claims 28-31 and 34-36. The Final Office Action of April 9, 2009 additionally objected to the amended title.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

While reference characters are used in the following summary to identify examples of claim elements that are shown in the drawings, it should be noted that the reference characters are included merely to ensure full compliance with the requirements of 37 C.F.R. § 41.37(c)(1)(v), and that their inclusion merely points to examples in the as-filed disclosure that do not limit the scope of any claim that remains pending in the above-referenced application. Rather, the scope of each claim is limited only by the plain language thereof, and includes the full scope of available equivalents to each recited element.

The subject matter presently claimed in pending claims 28-31 and 34-36 relates to semiconductor memory fabrication. (Specification, page 2, ¶ [0001]). Specifically, the invention presently claimed is a semiconductor memory device of smaller size through the use of container-configured capacitors (Specification, page 16, ¶ [0086]) and digit lines in a common vertical plane. (*See* Specification, page 19, ¶ [0099]).

With respect to independent claim 28, an integrated circuit is provided that comprises a semiconductor die (90). (Specification, page 16, ¶ [0085]). A plurality of memory cells are arranged in at least one array formed on the semiconductor die, each of the plurality of memory cells including at least one container-configured capacitor (102, 104) (Fig. 24; Specification, page 16 ¶ [0086]) having a storage node (110) (Fig. 24; Specification, page 16, ¶ [0087]) including a roughened outer surface in a substantially vertical dimension with respect to the semiconductor die. (*Id.*). A word line (e.g. 96) is formed substantially below the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the word

line. (Fig. 24; Specification, page 16, ¶ [0085]). A first digit line (124) is formed substantially above the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the first digit line. (Fig. 24; Specification, page 17, ¶ [0089]). A second digit line (D*) is formed substantially above the first digit line, wherein the second digit line and the first digit line are separated by an insulated dielectric material. (Fig. 27; Specification, page 19, ¶ [0097-99])

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The 35 U.S.C. § 103(a) rejections of claims 28, 29, 31 and 34 for being directed to subject matter which is allegedly unpatentable over the teachings of U.S. Patent 5,338,700 to Dennison et al. (hereinafter "Dennison") in view of U.S. Patent 5,378,908 to Chin et al. (hereinafter "Chin");

(B) The 35 U.S.C. § 103(a) rejection of claim 30 for being directed to subject matter which is allegedly unpatentable over the teachings of Dennison in view Chin, and further in view of U.S. Patent 5,838,038 to Takashima et al. (hereinafter "Takashima").

(C) The 35 U.S.C. § 103(a) rejections of claims 35-36 for being directed to subject matter which is allegedly unpatentable over the teachings of Dennison in view of Chin and further in view of U.S. Patent 5,610,418 to Eimori (hereinafter "Eimori").

(7) ARGUMENT

(A) Rejections Under 35 U.S.C. § 103(a)

(1) Authorities Relied Upon

To establish a *prima facie* case of obviousness the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. *In re Royka*, 490 F.2d 981, 985 (CCPA 1974); *see also* MPEP § 2143.03. Additionally, the Examiner must determine whether there is "an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1740-1741, 167 L.Ed.2d 705, 75 USLW 4289, 82 U.S.P.Q.2d 1385 (2007). Further, rejections on obviousness grounds "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id* at 1741, quoting *In re Kahn*, 441, F.3d 977, 988 (Fed. Cir. 2006). Finally, to establish a *prima facie* case of obviousness there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). Furthermore, the reason that would have prompted the combination and the reasonable expectation of success must be found in the prior art, common knowledge, or the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006); MPEP § 2144. Underlying the obvious determination is the fact that statutorily prohibited hindsight cannot be used. *KSR*, 127 S.Ct. at 1742; *DyStar*, 464 F.3d at 1367.

(2) Analysis

(i) Obviousness Rejection Based on Dennison in View of Chin

Claims 28, 29, 31 and 34 stand rejected for being directed to subject matter which is allegedly unpatentable over the teachings of Dennison in view of Chin.

Regarding claim 28, the Examiner admits that Dennison "fails to expressly [disclose] a device, further comprising a second digit line, where the second digit line and the first digit line are separated by an insulated dielectric material." Office Action, page 3, dated April 9, 2009.

The Examiner further asserts that:

> Chin discloses a device, comprising a second digit line (22) formed substantially above the first digit line, where the second digit line and the first digit line are separated by an insulated dielectric material (see Fig. 3) . . . [a] person having ordinary skill in the art . . . would have readily recognized the desirability and advantages of modifying Dennison as suggested by Chin, by employing a dielectric layer between the first and second digit lines. This cell arrangement would produce a wide effective area for the capacitor and improve the topology of the digit line contact area (Chin: col. 4, lines 59-68 and col. 5, lines 1-10). (Office Action, page 4, dated April 9, 2009.)

The Appellants respectfully disagree with the Examiner's characterization of Chin. Specifically, Chin does not once define or describe element 22 other than its mere presence in Figure 3. The Appellants respectfully assert that the unreferenced element 22 cannot reasonably be interpreted to be a digit line sufficient to provide an enabling disclosure sufficient to lead one skilled in the art to arrive at the claimed invention based on the teachings of Dennison and Chen.

Furthermore, in addition to not teaching anything concerning a second digit line, the alleged motivation offered by the Examiner for modifying Dennison with Chin does not correlate with any description of a second digit line. Rather, Chin teaches that the cell arrangement "has a wide effective area for the capacitor . . . **because** the storage poly-silicon for **capacitor is formed** with an enough **thickness** over the field oxide layer 4, as well as the exposed area of the storage poly layer 13 is increased by causing the undercut just below the boundary region of the storage layer to bring about." (Chin, col. 4, lines 60-66, emphasis added). Chin also teaches that "[s]ince the storage poly layer to be the **capacitor** electrode **is formed** not only thick in the region over the field oxide layer, but also **shallowly in the contact region of the bit line**, the effective area of the capacitor increases and the topology of the bit line contact area is improved." (Chin, col. 5, lines 5-10, emphasis added).

Therefore, the alleged motivation and advantages offered by the Examiner to support the rejection appear to actually be due to the way in which the capacitor is formed, and not from any reference to the existence of a second digit line or the placement of a second digit line in relation to a first digit line. Chin teaches that these advantages are due to the capacitor itself being formed thick over the field oxide layer and shallowly in the contact region of the bit line.

Therefore, the Appellants respectfully assert that neither Dennison or Chen, individually nor in combination teach "a second digit line formed substantially above the first digit line, wherein the second digit line and the first digit line are separated by an insulated dielectric material" as is recited by independent claim 28.

Claims 29, 31 and 34 depend from independent claim 28 which is allowable for the reasons asserted above. Therefore, at least by virtue of their dependence from an allowable claim, claims 29, 31 and 34 are also allowable.

(ii) Obviousness Rejections Based on Dennison in View of Chin and Further in View of Takashima

Claim 30 stands rejected for being directed to subject matter which is allegedly unpatentable over the teachings of Dennison in view Chin, and further in view of Takashima.

Claim 30 depends from independent claim 28 which is allowable for the reasons asserted above. Therefore, at least by virtue of its dependence from an allowable claim, claim 30 is also allowable.

(iii) Obviousness Rejections Based on Dennison in View of Chin and Further in View of Eimori

Claims 35-36 stand rejected for being directed to subject matter which is allegedly unpatentable over the teachings of Dennison in view of Chin and further in view of Eimori.

Claims 35-36 depend from independent claim 28 which is allowable for the reasons asserted above. Therefore, at least by virtue of their dependence from an allowable claim, claims 35-36 are also allowable.

(8) CLAIMS APPENDIX

A copy of claims 28-31 and 34-36 is appended hereto as Appendix A. Claims 28-31 and 34-36 are involved in the Appeal.

(9) EVIDENCE APPENDIX

There is no evidence appendix.

(10) RELATED APPEALS APPENDIX

There is no related appeals appendix. A prior appeal (Appeal No. 2007-3528) of canceled claims 6-10, 18, 19, 22, 23, 25, and 26 was previously filed but the canceled claims are not part of the pending claims being appealed.

CONCLUSION

Appellant respectfully requests the reversal of the rejections of currently pending claims 28-31, and 34-36 for the reasons set forth above.

Respectfully submitted,

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APPENDIX A

Claims Appendix

Claims 28-31, and 34-36

U.S. Patent Application No. 08/530,661

Filed September 20, 1995

28. (Previously Presented) An integrated circuit comprising:

a semiconductor die;

a plurality of memory cells arranged in at least one array formed on the semiconductor die, each of the plurality of memory cells including at least one container-configured capacitor having a storage node including a roughened outer surface in a substantially vertical dimension with respect to the semiconductor die;

a word line formed substantially below the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the word line;

a first digit line formed substantially above the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the first digit line; and

a second digit line formed substantially above the first digit line, wherein the second digit line and the first digit line are separated by an insulated dielectric material.

29. (Previously Presented) The integrated circuit of claim 28, further comprising circuitry formed on the semiconductor die and coupled to the memory cells for permitting data to be written to and read from the plurality of memory cells.

30. (Previously Presented) The integrated circuit of claim 28, wherein the memory cells are formed with a minimum capable photolithographic feature dimension, and a single one of the memory cells consumes an area of no more than eight times the square of the minimum capable photolithographic feature dimension.

31. (Previously Presented) The integrated circuit of claim 28, further comprising a conductive isolation line formed substantially below the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the conductive isolation line.

34. (Previously Presented) The integrated circuit of claim 28, wherein the memory cells are dynamic random access memory cells.

35. (Previously Presented) The integrated circuit of claim 28, wherein at least 16,000,000 to 17,000,000 functional and operably addressable memory cells are formed on the semiconductor die.

36. (Previously Presented) The integrated circuit of claim 35, wherein all the functional and operably addressable memory cells formed on the semiconductor die have a combined area on the semiconductor die that is no greater than 14 mm^2.